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Title: PACKAGING OF ELECTRONIC CHIPS WITH AIR-BRIDGE STRUCTURES
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PACKAGING OF ELECTRONIC CHIPS WITH AIR-BRIDGE STRUCTURES

Field of the Invention

This invention relates to the packaging of electronic chips, and more particularly to the packaging of electronic chips having air-bridge structures.

Background of the Invention

As the density of devices, such as resistors, capacitors, and transistors, in an integrated circuit is increased, the distance between the signal carrying conductors is decreased, and the capacitive coupling between the conductors is increased. Several problems result from the increased capacitive coupling. First, the increased capacitive coupling reduces the rate at which information can be transferred along each of the signal carrying conductors. Second, the increased capacitive coupling between the signal carrying conductors reduces the noise margin on the conductors. In the worst case, a signal on one signal carrying conductor is capacitively coupled to an adjacent signal carrying conductor, and the information on the adjacent conductor is destroyed. Since it is desirable to avoid destroying information, it is also desirable to reduce the capacitive coupling between the signal carrying conductors of an integrated circuit.

In an integrated circuit, decreasing the dielectric constant of an insulator that separates two adjacent signal carrying conductors reduces the capacitive coupling between the two adjacent signal carrying conductors. Silicon dioxide is the most commonly used insulator in the fabrication of integrated circuits and has a relatively high dielectric constant of about four. Carbon dioxide has a smaller dielectric constant than silicon dioxide, so replacing silicon dioxide with carbon dioxide reduces the capacitive coupling between the two adjacent conductors. Unfortunately, the thermal conductivity of carbon dioxide is much less than the thermal conductivity of silicon dioxide. This lower thermal conductivity causes a reduction in the rate at which heat is conducted away from an integrated circuit chip that employs a carbon dioxide insulator, which can result in the catastrophic failure of the integrated circuit.

Air has a dielectric constant of one, which is less than the dielectric constant of carbon dioxide and much less than the dielectric constant of silicon dioxide. Replacing silicon dioxide with air in an integrated circuit reduces the capacitive coupling between signal carrying conductors. Air bridge structures, which are structures consisting primarily of signal carrying conductors surrounded by air in an integrated circuit, are fabricated to reduce the dielectric constant in the conductive structures of an integrated circuit. Unfortunately, since, in an air bridge structure, the signal carrying conductors are no longer embedded in a layer of silicon dioxide, the structural integrity of the integrated circuit is decreased. This problem is especially significant when an integrated circuit fabricated using air bridge structures is packaged as a flip chip,

For these an other reasons there is a need for the present invention.

Summary of the Invention

The above mentioned problems with air bridge structures, closely spaced conductors, silicon dioxide insulators and other problems are addressed by the present invention and will be understood by reading and studying the following specification.

A circuit assembly for fabricating an air bridge structure and a method of fabricating an integrated circuit package capable of supporting an air bridge structure is disclosed. A circuit assembly comprises an electronic chip and a conductive structure embedded in a plurality of materials having a plurality of vaporization temperatures. The plurality of materials are formed on the electronic chip and the conductive structure is coupled to the electronic chip.

A method of forming an air bridge structure comprising a plurality of operations is also disclosed. First, a support structure including interstices is formed on an electronic chip. Next, the interstices of the support structure are filled with a material having a vaporization temperature that is less than the vaporization temperature of the support structure. Conductive structures are embedded in the support structure and the material, and a connective structure is mounted on the support structure. Finally, the material is removed from the support structure.

Brief Description of the Drawings

Figure 1 is a cutaway perspective view of some embodiments of an integrated circuit assembly employing a ribbed support structure of the present invention.

Figure 2A is a cross-sectional view of the integrated circuit assembly of Figure 1 along the section line 2.

Figure 2B is a cross-sectional view of the integrated circuit assembly of Figure 1 along the section line 3.

Figure 3 is a perspective view of some embodiments of an integrated circuit assembly of the present invention employing a post support structure.

Figure 4 is a perspective view of some embodiments of an integrated circuit assembly mounted on a substrate.

Figure 5A is a simplified schematic of an air-bridge structure supported by conductive posts.

Figure 5B is a simplified schematic of an air-bridge structure supported by insulating posts.

Figure 6 is a block diagram of a computer system suitable for use in connection with the present invention.

Detailed Description of the Preferred Embodiments

In the following detailed description of the preferred embodiments, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific preferred embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that logical, mechanical and electrical changes may be made without departing from the spirit and scope of the present inventions. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims.

Figure 1 is a cutaway perspective view of some embodiments of integrated circuit assembly 100 of the present invention. Integrated circuit assembly 100, in one

embodiment, includes electronic chip 103, and material layer 106, comprising ribbed support structure 109, fill material 112, conductive structure 115, and interstices 116. In an alternate embodiment, integrated circuit assembly 100 also includes controlled collapse chip connection (C4) structure 118 comprising insulation layer 121, vaporization plug 124, and conductive elements 127 and 130.

Integrated circuit assembly 100 is not limited to use in connection with a particular type of electronic chip 103. Memory chips, such as a dynamic random access memory (DRAM) chips, static random access memory (SRAM) chips, read-only-memory (ROM) chips, and random access memory (RAM) chips, microprocessor chips, logic chips, digital signal processing chips, analog signal processing chips, and application specific integrated circuit (ASIC) chips can all be used in connection with integrated circuit assembly 100.

Material layer 106 is fabricated on the surface of electronic chip 103, and has a plurality of vaporization temperatures. In one embodiment, material layer 106 is fabricated from a plurality of materials in which each of the plurality of materials has a different vaporization temperature.

Material layer 106 includes a structural component, such as ribbed structure 109, and a non-structural component, such as fill material 112. An advantage of using a structural component in the present invention is that the structural component is easily modified to support flip-chip mounting or silicon on substrate mounting of electronic chip 103, without interfering with the layout of the air-bridge structures. Ribbed structure 109 is designed to support the entire weight of electronic chip 103, if electronic chip 103 is mounted using a C4 or flip-chip interconnect. If electronic chip 103 is not mounted using as a C4 or flip-chip interconnect, then the design of ribbed structure 109 is only required to support long run air bridge structures. Ribbed structure 109, in one embodiment, is fabricated by forming a layer of inorganic material, such as SiO_2, Si_3N_4, or a low temperature SiO_2, on the surface of electronic chip 103. The layer of inorganic material is formed to a depth equal to the distance between the surface of electronic chip 103 and the first wiring layer of electronic chip 103. The surface of the layer of inorganic material is patterned and etched to form ribbed structure 109.

Fill material 112 is a non-structural component, and in one embodiment, is a polymer, such as a photoresist or a polyimide. Preferably, fill material 112 is carbon, which has a vaporization temperature of about 400 degrees centigrade, and is deposited in interstices 116 or the etched areas of ribbed structure 109 by sputtering. Fill material 112 is patterned and etched to form a template for the vertical wiring vias and the horizontal interconnect paths of conductive structure 115. In one embodiment, conductive structure 115 is fabricated using the dual damascene process. ("Process for Fabricating Multi-Level Integrated Circuit Wiring Structure from a Single Metal Deposit", John E. Cronin and Pei-ing P. Lee, United States Patent 4,962,058, October 9, 1990, is incorporated by reference.) Alternatively, a single damascene or a subtractive etch process sequence is used to produce conductive structure 115. Conductive structure 115 is formed by depositing a conductive material, such as aluminum, gold, silver, or copper, or an alloy of aluminum, gold, silver, or copper, in the vertical wiring vias and conductive interconnect paths of the template formed in fill material 112. The conductive vias couple conductive structure 109 to electronic chip 103. Excess conductive material is removed by a planarizing process, such as chemical mechanical polishing (CMP), applied to the surface of fill material 112 and ribbed structure 109. After CMP, the surface of fill material 112, ribbed structure 109, and conductive structure 115, including the conductive vias and conductive interconnects, are ready for coupling to C4 structure 118.

Variations of the process described above include fabricating material layer 106 from an organic material or a mix of organic materials and inorganic materials, and patterning and etching the surface of material layer 106 to form a post structure. In addition, the process described for forming air bridge structures and support structures can be repeated to form as many wiring levels as required for the design of a particular electronic chip 103.

C4 structure 118, comprising insulation layer 121, vaporization plug 124, and conductive elements 127, is formed above ribbed structure 109 and fill material 112. Insulation layer 121 is the base of C4 structure 118 and is fabricated from an insulator, such as SiO_2 or Si_3N_4. After forming insulation layer 121, vias are patterned and etched at via sites 127 and 130. A conductor, such as aluminum, gold, copper, or silver, or an

alloy of aluminum, gold, copper, or silver, is deposited to fill via sites 127 and 130, and the metal is polished back to the surface of ribbed support structure 109 and fill material 112. Finally, a vaporization plug site is etched in insulation layer 121, and a fill material 112, such as carbon, is deposited to form vaporization plug 124. Any excess carbon is removed by polishing back the carbon to the surface of ribbed structure 109 and fill material 112.

Integrated circuit assembly 100 is placed in a furnace to vaporize fill material 112, leaving air bridge-structure 115, C4 structure 118, and electronic chip 103. In one embodiment, the furnace has an O_2 atmosphere heated to about 400 degrees centigrade. In an alternate embodiment, integrated circuit assembly 100 is mounted as a flip chip on a substrate prior to vaporizing fill material 112.

Figure 2A is a cross-sectional view along the section line 2 of the integrated circuit assembly of Figure 1. Conductive structure 115 is formed in and above fill material 112. After fill material 112, which fills interstices 116 formed by ribbed support structure 109, is vaporized, conductive structure 115 is surround by a dielectric having a dielectric constant of about 1.

Figure 2B is a cross-sectional view along the section line 3 of the integrated circuit assembly of Figure 1. Support structure 109 having interstices 116 filled with fill material 112 is formed on electronic chip 103. Vaporization plug 124 is formed in fill material 112 and C4 structure 118. In one embodiment, vaporization plug 124 is fabricated from carbon. After heating integrated circuit assembly 100 in an O_2 atmosphere at a temperature of about 400 degrees centigrade, carbon fill material 112 and vaporization plug 124 are vaporized and the gas produced by the vaporization process expands through vaporization plug 124.

Figure 3 is a perspective view of some alternate embodiments of an integrated circuit assembly 300. Integrated circuit assembly 300 comprises electronic chip 303, a plurality of post support structures 306, connective structure 309, and conductive structure 312.

Integrated circuit assembly 300 is not limited to use in connection with a particular type of electronic chip 303. The electronic chips described as suitable for use

in connection with integrated circuit assembly 100 of Figure 1 are also suitable for use in connection with integrated circuit assembly 300.

The plurality of post support structures 306, in one embodiment, is formed from an inorganic material, such as SiO_2 or Si_3N_4. The processes described above for fabricating ribbed support structures 109 of Figure 1 can be applied to the fabrication of post support structures 306. Alternatively, the plurality of support structures 306 are formed from a conductor, such as aluminum, silver, gold or copper, or an alloy of aluminum, silver, gold or copper. When fabricated from a conductor or an alloy of a conductor, the plurality of post support structures 306 are formed on an insulating base 315 to ensure that the plurality of post support structures 306 do not directly couple to, load, or otherwise electronically interfere with the operation of the circuits formed on electronic chip 303.

To fabricate the plurality of post support structures 306 from a conductor, a layer of material is formed above electronic chip 303. In one embodiment, the layer of material is an organic material, such as carbon. Alternatively, the layer of material is an organic polymer. The layer of material is patterned and etched to form a template for the first level vertical wiring and the plurality of post support structures 306. The template for the vertical wiring and the plurality of post support structures 306 are filled with a conductive material to form the plurality of support structures 306 and the vertical wiring for conductive structure 312. Excess conductive material on the surface of the layer of material deposited above electronic chip 303 is removed by chemical mechanical polishing or a similar planarizing process. An advantage of forming post support structures 306 from a conductor is that post support structures 306 provide a thermally conductive path to the C4 surface.

To form a first level air-bridge conductive segment, a horizontal pattern is patterned and etched. A conductive material, such as gold, copper, aluminum, or silver, or an alloy of gold, copper, aluminum, or silver, is deposited to fill the etched pattern. Excess conductive material is planarized back to the level of the surface of the organic material. The operations described above for forming an air-bridge level are repeated until the fabrication of the final air-bridge level is completed.

After completion of the fabrication of the final air-bridge level, the support structure for the C4 contacts is formed from a layer of SiO_2 or other insulating material. The layer is patterned and etched to leave holes for vertical wiring to the positions of the C4 contacts. A layer of metal is applied to the surface of the SiO_2 and the surface is planarized back to the oxide surface leaving the vertical metal conductors flush with the oxide. This vertical wiring level connects the C4 contacts to the last air-bridge level. Additional openings are etched in the oxide such that all the interior carbon or polymer areas are accessible.

The C4 contacts on the surface of electronic chip 303 are reflowed in an H_2 atmosphere. Electronic chip 303 is flipped and the C4 contacts are joined to a substrate in an H_2 atmosphere. The assembly is placed in a furnace having an O_2 atmosphere at approximately 400 degrees centigrade and the carbon is reduced to gaseous CO_2. If a polymer is used as the fill material instead of the carbon, the polymer is also removed using an O_2 plasma.

If a hermetic packaging is used, the package is back filled with helium to improve the thermal properties of the assembly. If a heat sink is required, it is attached prior to the removal of the carbon support structure.

Figure 4 is a perspective view of some embodiments of integrated circuit assembly 400. Integrated circuit assembly 400 comprises substrate 403, C4 connective structure 406, electronic chip 409, a plurality of post support structures 412, air-bridge conductive structure 415, and heat sink 418. In assembling integrated circuit assembly 400, electronic chip 409 is fabricated for flip chip mounting using C4 structure 406. A plurality of post support structures 412 and an air-bridge structure 415 are fabricated on electronic chip 406. The plurality of post support structures 412 support electronic chip 409 when mounted as a flip-chip on substrate 403. Heat sink 418 assists in cooling electronic chip 409 by conducting heat away form electronic chip 409. If the fill material in which connective structure 406 is fabricated is not removed from integrated circuit assembly 400 prior to mounting electronic chip 409 on substrate 403, the fill material is removed by heating integrated circuit assembly 400. In one embodiment, integrated circuit assembly 400 is heated in an O_2 atmosphere at 400 degrees centigrade. The fill

material is vaporized, and air-bridge conductive structure 415 is surround by air having a dielectric constant of about 1. To improve the cooling characteristics of integrated circuit assembly 400, substrate 403 is hermetically sealed and filled with helium or a helium rich gas.

Figure 5A is a simplified schematic of air-bridge structure 500 supported by conductive posts 503 and 506. Long run air-bridge conductive structure 509 couples electronic devices embedded in electronic chip 512. Conductive posts 503 and 506 support long run air-bridge conductive structure 509 and C4 connective structure 515. Conductive posts 503 and 506 are terminated in insulators 518 and 521 at the surface of electronic chip 512. An advantage fabricating conductive support posts 503 and 506 from a conductive material, such as aluminum, copper, gold, or silver, or an alloy of aluminum copper, gold, or silver is that conductive support posts 503 and 506 are fabricated at the same time that air-bridge conductive structure 509 is fabricated.

Figure 5B is a simplified schematic of air-bridge structure 550 coupling devices embedded in electronic chip 553 and supported by insulating posts 556 and 559. Insulating posts 556 and 559, in one embodiment, are fabricated from silicon dioxide. Insulating posts 556 and 559 support long run air bridge structure 562 and support C4 connective structure 565. The fabrication of long run air bridge structure 562 and C4 connective structure 565 are described above in connection with Figure 3 and Figure 4.

Figure 6 a block diagram of a computer system 400 suitable for use in connection with the present invention. System 600 comprises processor 605 and memory device 610, which includes an integrated circuit assembly of one or more of the types described above in conjunction with Figures 1-3. Memory device 610 comprises memory array 615, address circuitry 620, and read circuitry 630, and is coupled to processor 605 by address bus 635, data bus 640, and control bus 645. Processor 605, through address bus 635, data bus 640, and control bus 645 communicates with memory device 610. In a read operation initiated by processor 605, address information, data information, and control information are provided to memory device 610 through busses 635, 640, and 645. This information is decoded by addressing circuitry 620, including a row decoder and a column decoder, and read circuitry 630. Successful completion of the read operation

results in information from memory array 615 being communicated to processor 605 over data bus 640.

Conclusion

An integrated circuit assembly having air-bridge structures and a method for manufacturing an integrated circuit assembly having air-bridge structures has been described. An integrated circuit assembly includes structural components that protect the air-bridge structures during flip-chip mounting. A method of fabricating an electronic chip compatible with flip-chip mounting techniques includes the fabrication of ribbed support structures and post support structures. The support structures are fabricated from either insulating or conductive materials.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. Therefore, it is intended that this invention be limited only by the claims and the equivalents thereof.

What is claimed is:

1. An integrated circuit assembly comprising:

an electronic chip; and

a conductive structure embedded in a material layer having a plurality of vaporization temperatures, the material layer is formed on the electronic chip and the conductive structure is coupled to the electronic chip.

2. The integrated circuit assembly of claim 1, wherein the electronic chip is a memory chip.

3. The integrated circuit assembly of claim 2, wherein the memory chip is a dynamic random access memory chip.

4. The integrated circuit assembly of claim 1, wherein the conductive structure is fabricated from copper.

5. The integrated circuit assembly of claim 1, wherein at least one of the plurality of vaporization temperatures is about 400 degrees centigrade.

6. An integrated circuit assembly comprising:

an electronic chip; and

a conductive structure embedded in a plurality of materials, each of the plurality of materials having a different vaporization temperature, the plurality of materials is formed on the electronic chip and the conductive structure is coupled to the electronic chip.

7. The integrated circuit assembly of claim 6, wherein the electronic chip is an analog signal processing chip.

8. The integrated circuit assembly of claim 6, wherein at least one of the plurality of materials is silicon dioxide.

9. The integrated circuit assembly of claim 6, wherein at least one of the plurality of materials is carbon.

10. An integrated circuit assembly comprising:

an electronic chip; and

a conductive structure embedded in a material layer having a structural component having a structural vaporization temperature and a non-structural component having a non-structural vaporization temperature less than the structural vaporization temperature, the material layer is formed on the electronic chip and the conductive structure is coupled to the electronic chip.

11. The integrated circuit assembly of claim 10, wherein the electronic chip is a digital signal processor.

12. The integrated circuit assembly of claim 10, wherein the structural component is fabricated from silicon dioxide.

13. The integrated circuit assembly of claim 12, wherein the silicon dioxide is a low temperature silicon dioxide.

14. The integrated circuit assembly of claim 10, wherein the non-structural component is fabricated from carbon.

15. The integrated circuit assembly of claim 10, wherein the non-structural component is fabricated from a polymer.

16. The integrated circuit assembly of claim 15, wherein the polymer is a photoresist.

17. The integrated circuit assembly of claim 10, wherein the electronic chip is comprised of logic circuits.

18. An integrated circuit assembly comprising:

an electronic chip;

a support structure mounted on the electronic chip, the support structure having an interstice and a vaporization temperature;

a material filling the interstice, the material having a vaporization temperature that is less than the vaporization temperature of the support structure;

a connective structure mounted on the support structure; and

a conductive structure capable of coupling the electronic chip to the connective structure, the conductive structure embedded in the support structure and the material.

19. The integrated circuit assembly of claim 18, wherein the electronic chip is a dynamic random access memory chip.

20. The integrated circuit assembly of claim 18, wherein the support structure is fabricated from silicon dioxide.

21. The integrated circuit assembly of claim 18, wherein the support structure is a ribbed structure.

22. The integrated circuit assembly of claim 18, wherein the material is carbon dioxide.

23. The integrated circuit assembly of claim 18, wherein the connective structure is a controlled collapse chip connection (C4) structure.

24. The integrated circuit assembly of claim 18, wherein the conductive structure is fabricated from a copper alloy.

25. An integrated circuit assembly comprising:

an electronic chip; and

a conductive structure including a support structure, the conductive structure having a vaporization temperature and the conductive structure including the support structure is embedded in a material layer having a vaporization temperature less than the vaporization temperature of the conductive structure, the material layer is formed on the electronic chip and the conductive structure is coupled to the electronic chip.

26. The integrated circuit assembly of claim 25, wherein the electronic chip is a microprocessor.

27. An integrated circuit memory device comprising:

an electronic memory chip; and

a ribbed structure mounted on the electronic memory chip and capable of protecting an air-bridge structure and supporting a C4 structure.

28. The integrated circuit assembly of claim 27, wherein the ribbed structure is fabricated from an inorganic insulator.

29. The integrated circuit assembly of claim 27, wherein the ribbed structure is fabricated from an organic material.

30. The integrated circuit assembly of claim 27, wherein the ribbed structure is fabricated from of a mix of organic and inorganic materials.

31. An integrated circuit assembly comprising:

an electronic chip; and

a post structure mounted on the electronic chip and capable of protecting an air-bridge structure and supporting a C4 structure.

32. The integrated circuit assembly of claim 31, wherein the post structure is fabricated from the same material as the air-bridge structure.

33. The integrated circuit assembly of claim 31, wherein the post structure is mounted on an insulating base formed on the electronic chip.

34. The integrated circuit assembly of claim 31, wherein the post structure is fabricated from an insulator.

35. The integrated circuit assembly of claim 31, wherein the insulator is silicon dioxide.

36. The integrated circuit assembly of claim 31, wherein the post structure is fabricated from a polymer.

37. The integrated circuit assembly of claim 36, wherein the polymer is polyimide.

38. An integrated circuit assembly comprising:

an electronic chip including a plurality of electronic devices;

a plurality of conductive segments capable of interconnecting the plurality of electronic devices, each of the plurality of conductive segments having a surface area in contact with a material having a dielectric constant of about 1;

a C4 connection coupled to the electronic chip through the plurality of conductive segments; and

a substrate coupled to the C4 connection.

39. The integrated circuit assembly of claim 38, wherein the integrated circuit assembly is hermetically sealed.

40. The integrated circuit assembly of claim 39, wherein the integrated circuit assembly is back filled with helium.

41. The integrated circuit assembly of claim 39, wherein the integrated circuit assembly is back filled with a helium rich gas mixture.

42. The integrated circuit assembly of claim 38, wherein the material is air.

43. The integrated circuit assembly of claim 38, wherein the material is a foam.

44. The integrated circuit assembly of claim 38, further comprising a heat sink coupled to the electronic chip.

45. The integrated circuit assembly of claim 44, wherein the integrated circuit assembly is hermetically sealed.`

46. The integrated circuit assembly of claim 45, wherein the integrated circuit assembly is back filled with helium.

47. A computer system comprising:

a processor;

a memory device having a plurality of circuit devices, the memory device coupled to the processor; and

an air-bridge structure and a support structure fabricated on the memory device, the air-bridge structure capable of coupling at least two of the plurality of circuit devices and the support structure capable of supporting the memory device mounted as a flip chip.

48. The computer system of claim 47, wherein the air-bridge structure is embedded in a dielectric having a dielectric constant of about 1.

49. The computer system of claim 47, wherein the support structure fabricated on the memory device is a ribbed support structure.

50. A method of constructing an integrated circuit comprising:

fabricating a plurality of electronic devices on a substrate;

embedding a wiring structure in a plurality of materials having a plurality of vaporization temperatures, the plurality of materials is located on the substrate and the wiring structure interconnects the plurality of electronic devices;

mounting the integrated circuit on a packaging substrate; and

removing at least one of the plurality of materials after the integrated circuit is mounted on the packaging substrate.

51. The method of claim 50, further comprising:

attaching a C4 structure to the integrated circuit prior to mounting the integrated circuit on the packaging substrate.

52. The method of claim 51, wherein removing at least one of the plurality of materials after the integrated circuit is mounted on the packaging substrate comprises:

heating the integrated circuit.

53. The method of claim 52, wherein heating the integrated circuit comprises:

placing the integrated circuit in a furnace having an oxygen atmosphere heated to about 400 degrees centigrade.

54. A method of forming an air bridge structure comprising:

forming a support structure having a support structure vaporization temperature and having interstices on an electronic chip;

filling the interstices of the support structure with a fill material having a vaporization temperature that is less than the support structure vaporization temperature;

embedding a conductive structure in the support structure and the material;

mounting a connective structure on the support structure; and

removing the fill material.

55. The method of claim 54, wherein forming a support structure having a support structure vaporization temperature and having interstices on an electronic chip comprises:

depositing a layer of silicon dioxide on the electronic chip; and

etching the layer of silicon dioxide to form the support structure having interstices.

56. A method of forming an air bridge structure comprising:

forming a support structure having interstices on an electronic chip;

filling the interstices of the support structure with a fill material having a vaporization temperature that is less than the vaporization temperature of the support structure;

embedding a conductive structure in the fill material;

mounting a connective structure on the support structure; and

vaporizing the fill material.

57. The method of claim 56, wherein filling the interstices of the support structure with a material having a vaporization temperature that is less than the vaporization temperature of the support structure comprises:

depositing a layer of carbon on the electronic chip.

58. The method of claim 57, wherein depositing a layer of carbon on the electronic chip comprises:

sputtering the layer of carbon on the electronic chip.

59. The method of claim 58, further comprising:

planarizing the layer of carbon.

60. A method of forming an air bridge structure comprising:

forming a material layer on an electronic chip;

embedding a conductive structure and a conductive support structure in the material layer, the conductive structure is capable of electronically coupling to the electronic chip; and

removing the material layer.

61. The method of claim 60, wherein embedding a conductive structure and a conductive support structure in the material layer comprises:

etching the material layer to form a plurality of vertical wiring vias and a plurality of vertical support vias;

etching a wiring pattern in the material layer; and

applying a conductive material to the plurality of vertical wiring vias, the plurality of vertical support vias, and the wiring pattern.

62. The method of claim 61, wherein removing the material comprises:

vaporizing the material.

63. The method of claim 62, wherein vaporizing the material comprises:

processing the integrated circuit assembly in a furnace having an oxygen atmosphere at a temperature of approximately 400 degrees centigrade.

64. A method of forming an air bridge structure comprising:

forming a material layer on an electronic chip;

embedding a conductive structure and a conductive support structure in the material layer, the conductive structure is capable of being electronically coupled to the electronic chip;

mounting a connective structure on the support structure; and

removing the layer material.

65. The method of claim 64, further comprising:

attaching a heat sink to the electronic chip.

66. A method of packaging an integrated circuit comprising:

fabricating an integrated circuit structure including a conductive structure and a ribbed support structure embedded in a fill material;

mounting C4 pads on the integrated circuit structure;

mounting the integrated circuit structure on a substrate;

removing the fill material; and

backfilling with a gas and hermetically sealing the substrate.

67. The method of claim 66, wherein the gas is helium.

68. The method of claim 66, wherein the fill material is carbon.

69. The method of claim 66, wherein the fill material is a high temperature polymer.

70. The method of claim 66, wherein the high temperature polymer is polyimide.

71. The method of claim 66, where the structural material is a metal.

72. The method of claim 71, wherein the metal is copper.

73. The method of claim 66, wherein the structural material is SiO_2.

74. The method of claim 66, wherein the structural material is Si_3N_4.

Abstract of the Disclosure

A circuit assembly for fabricating an air bridge structure and a method of fabricating an integrated circuit package capable of supporting a circuit assembly including an air bridge structure. A circuit assembly comprises an electronic chip and a conductive structure embedded in a plurality of materials having a plurality of vaporization temperatures. The plurality of materials is formed on the electronic chip and the conductive structure is coupled to the electronic chip. To fabricate the circuit assembly, a support structure, including interstices, is formed on an electronic chip. The interstices of the support structure are filled with a material having a vaporization temperature that is less than the vaporization temperature of the support structure. Conductive structures are embedded in the support structure and the material, and a connective structure is mounted on the support structure. Finally, the material is removed from the interstices by heating the circuit assembly.

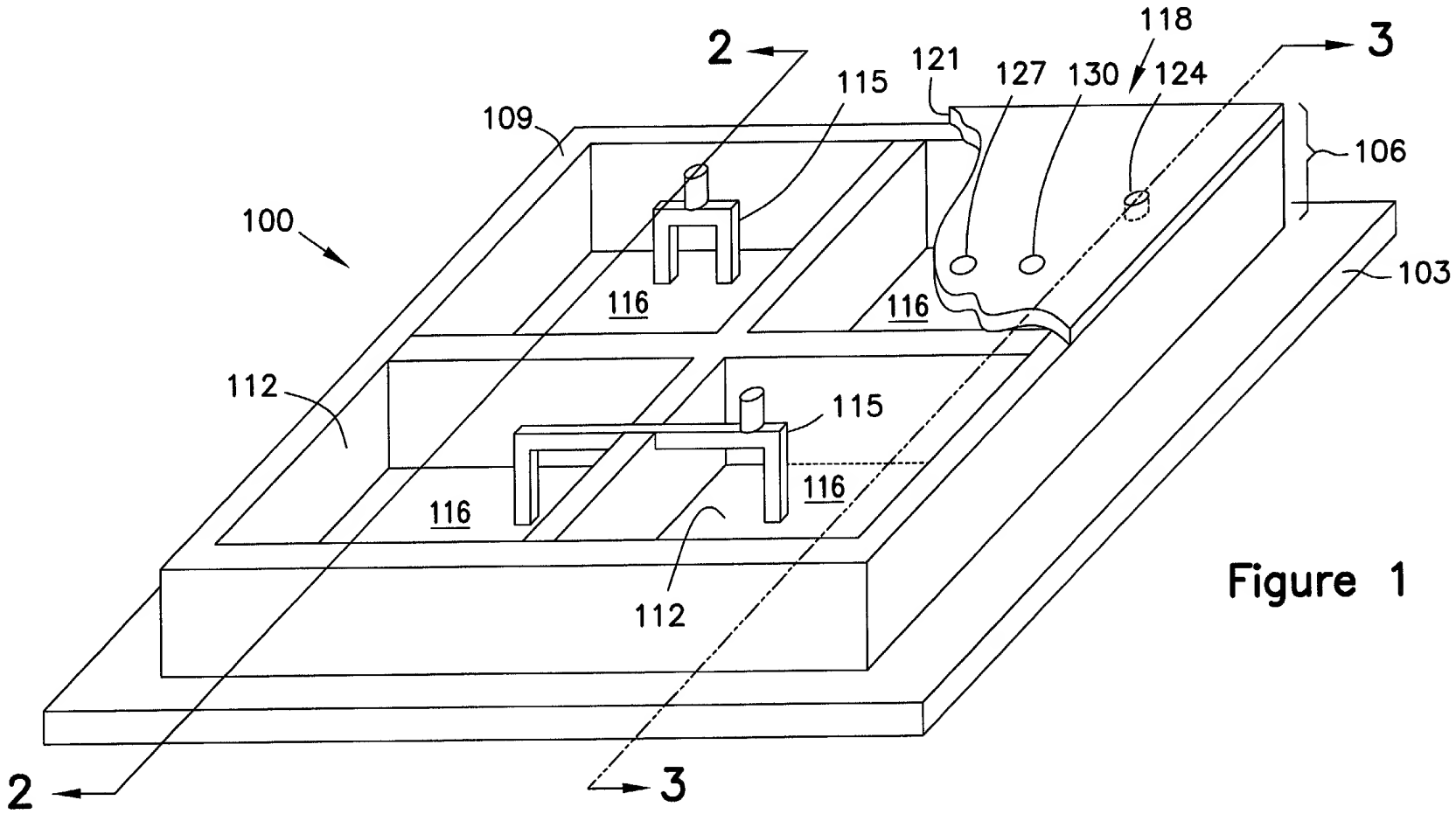
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Figure 1

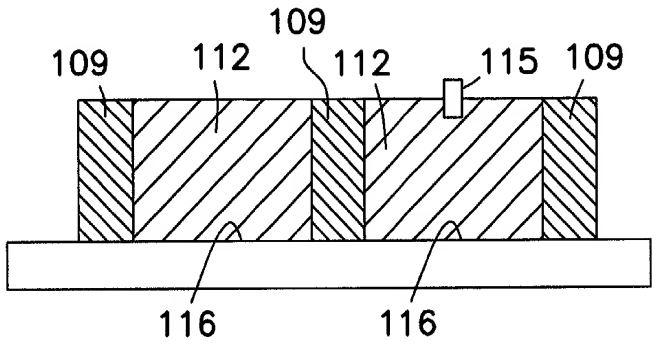


Figure 2A

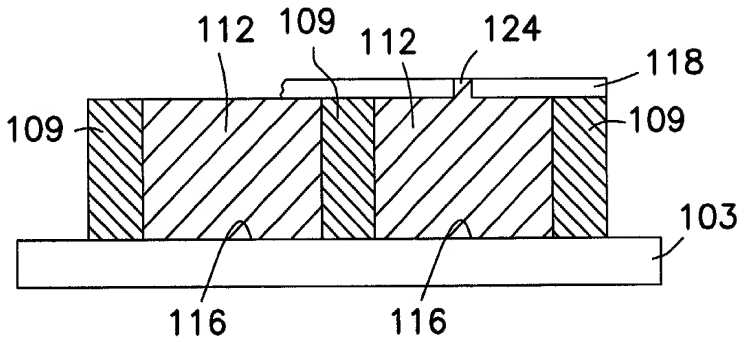


Figure 2B

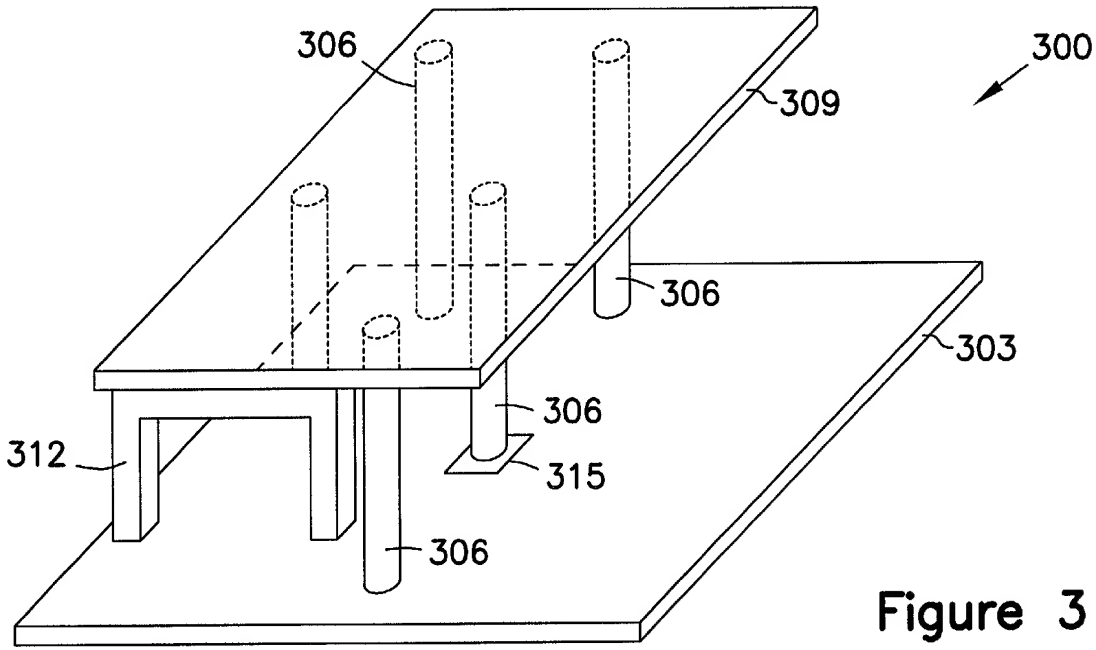


Figure 3

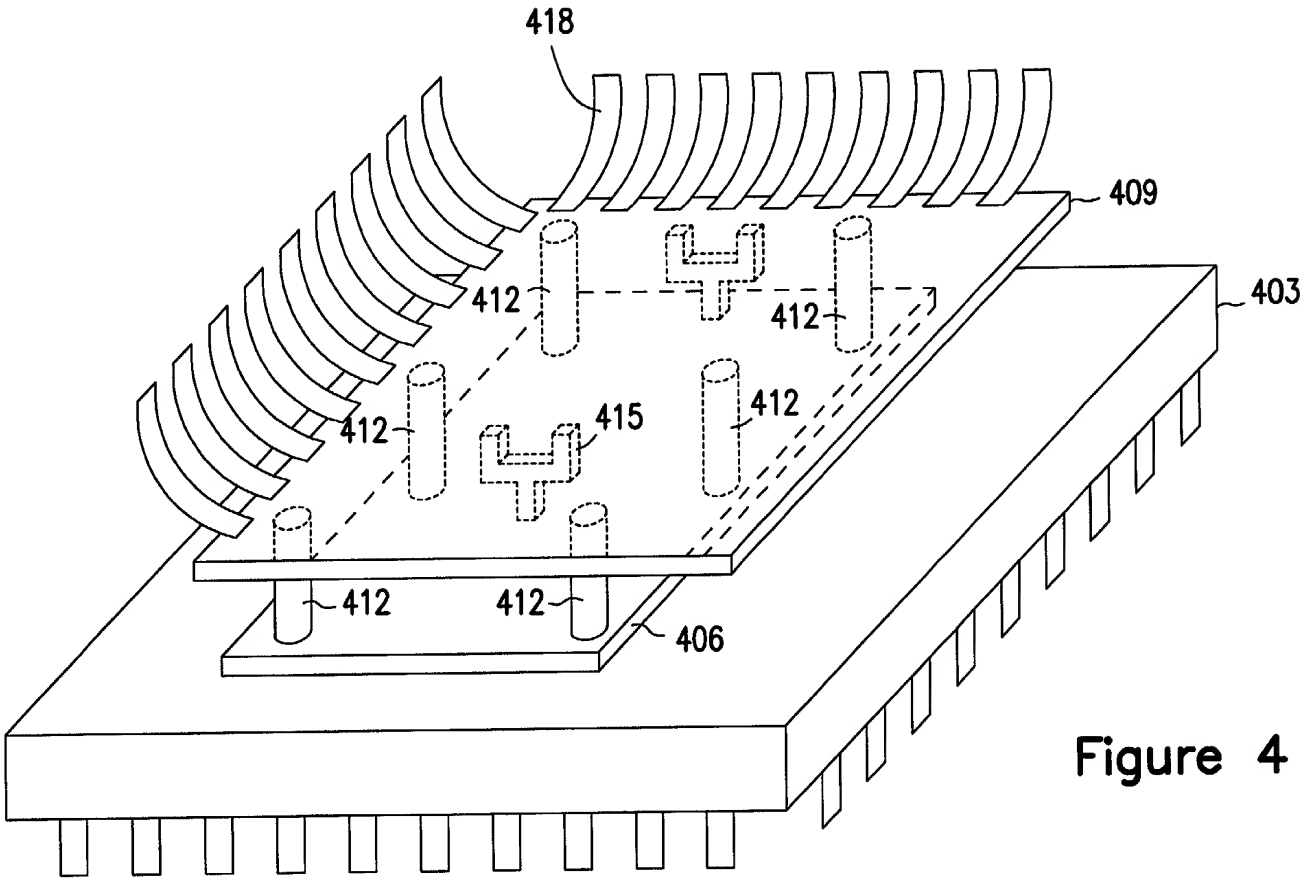


Figure 4

Figure 5A

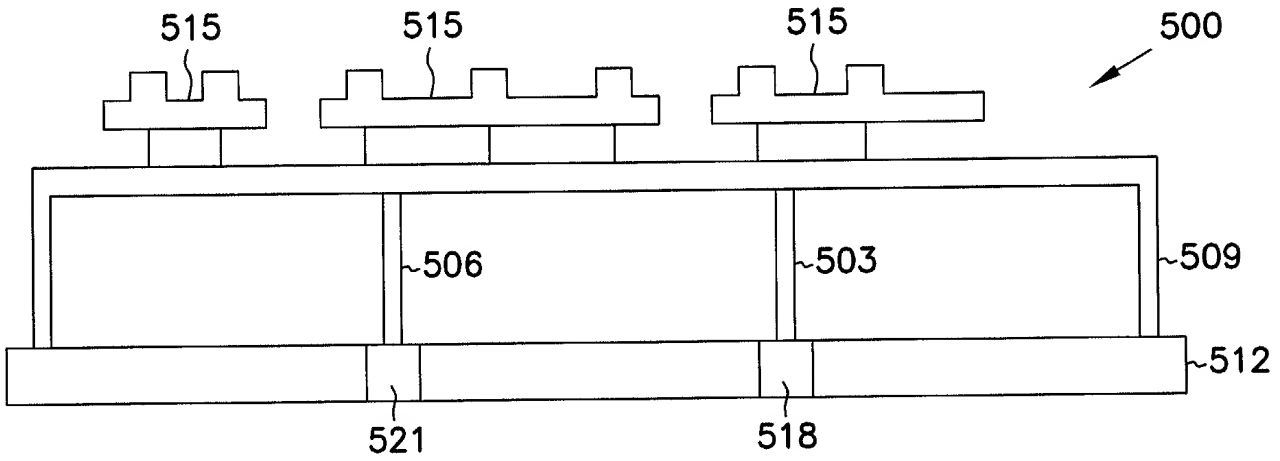
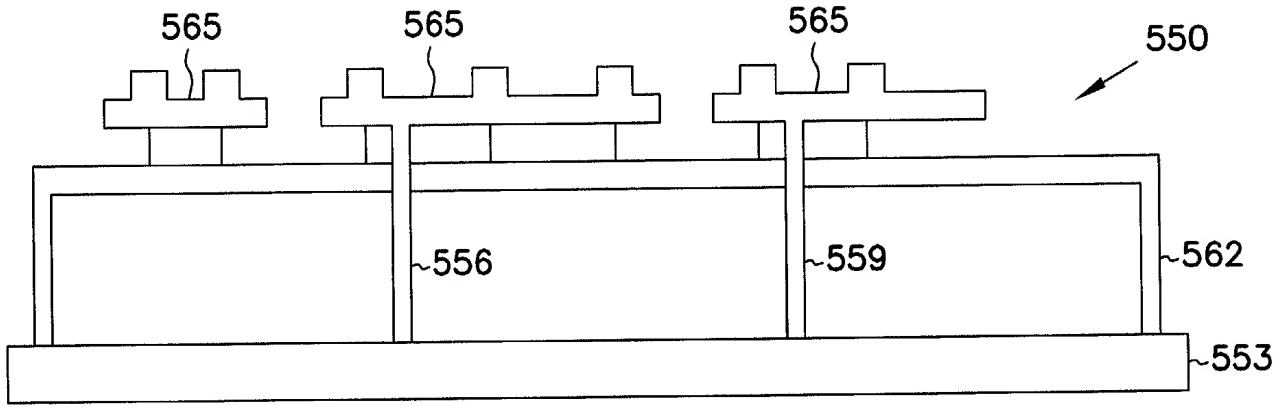


Figure 5B



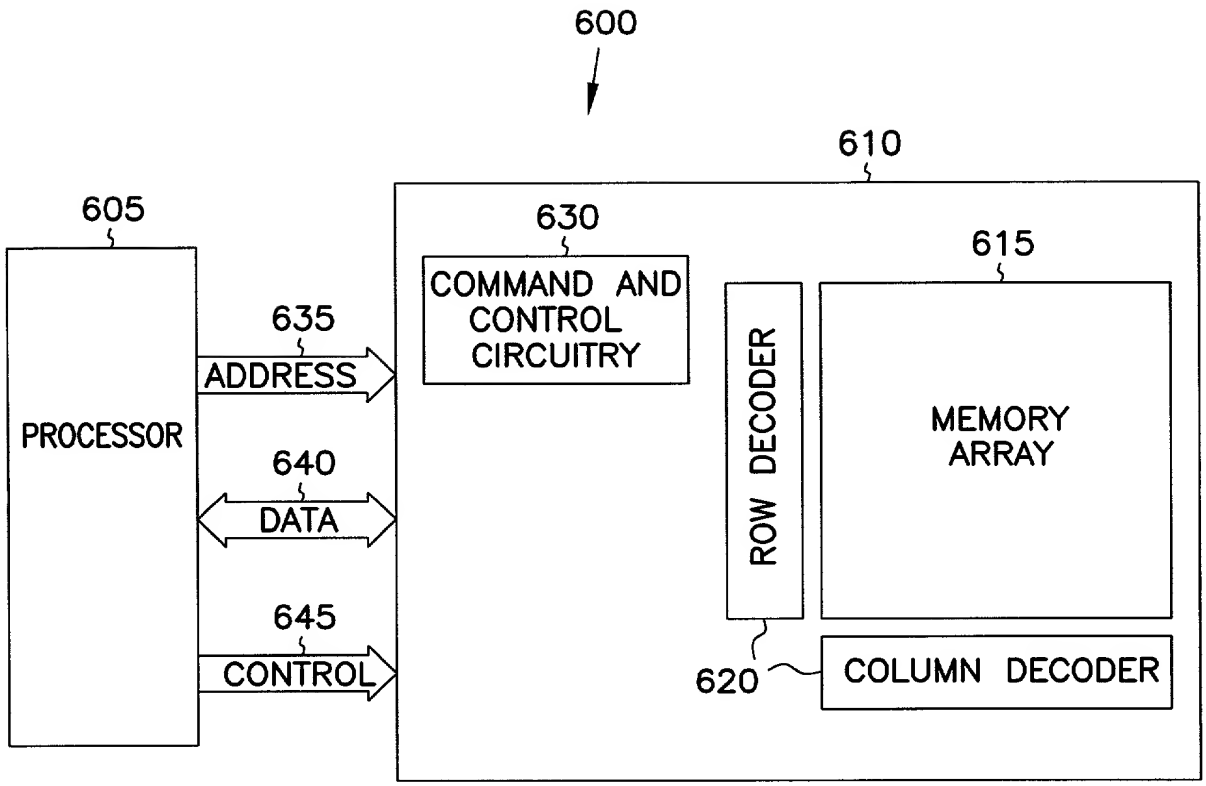

600
610
605
630
615
PROCESSOR
635
ADDRESS
COMMAND AND CONTROL CIRCUITRY
ROW DECODER
MEMORY ARRAY
640
DATA
645
CONTROL
620
COLUMN DECODER

Figure 6

S/N Unknown **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Paul A. Farrar	Examiner: Unknown	
Serial No.:	Unknown	Group Art Unit: Unknown	
Filed:	Herewith	Docket: 303.603US1	
Title:	PACKAGING OF ELECTRONIC CHIPS WITH AIR-BRIDGE STRUCTURES		

POWER OF ATTORNEY BY ASSIGNEE AND CERTIFICATE BY ASSIGNEE UNDER 37 CFR § 3.73(b)

Assistant Commissioner for Patents
Washington, D.C. 20231

Micron Technology, Inc., assignee of the entire right, title and interest in the above-identified application by assignment attached hereto, hereby appoints the attorneys and agents of the firm of SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A., listed as follows:

Adams, Gregory J.	Reg. No. P-44,494	Forrest, Bradley A.	Reg. No. 30,837	McCrackin, Ann M.	Reg. No. 42,858
Adams, Matthew W.	Reg. No. 43,459	Harris, Robert J.	Reg. No. 37,346	Nama, Kash	Reg. No. 44,255
Anglin, J. Michael	Reg. No. 24,916	Huebsch, Joseph C.	Reg. No. 42,673	Nelson, Albin J.	Reg. No. 28,650
Arora, Suneel	Reg. No. 42,267	Jurkovich, Patti J.	Reg. No. P-44,813	Nielsen, Walter W.	Reg. No. 25,539
Bianchi, Timothy E.	Reg. No. 39,610	Kalis, Janal M.	Reg. No. 37,650	Oh, Allen J.	Reg. No. 42,047
Billion, Richard E.	Reg. No. 32,836	Kaufmann, John D.	Reg. No. 24,017	Padys, Danny J.	Reg. No. 35,635
Black, David W.	Reg. No. 42,331	Klima-Silberg, Catherine I.	Reg. No. 40,052	Parker, J. Kevin	Reg. No. 33,024
Brennan, Thomas F.	Reg. No. 35,075	Kluth, Daniel J.	Reg. No. 32,146	Peacock, Gregg A.	Reg. No. P-45,001
Brooks, Edward J., III	Reg. No. 40,925	Lacy, Rodney L.	Reg. No. 41,136	Polglaze, Daniel J.	Reg. No. 39,801
Chu, Dinh C.P.	Reg. No. 41,676	Leffert, Thomas W.	Reg. No. 40,697	Prout, William F.	Reg. No. 33,995
Clark, Barbara J.	Reg. No. 38,107	Lemaire, Charles A.	Reg. No. 36,198	Schwegman, Micheal L.	Reg. No. 25,816
Dahl, John M.	Reg. No. P-44,639	Litman, Mark A.	Reg. No. 26,390	Sieffert, Kent J.	Reg. No. 41,312
Drake, Eduardo E.	Reg. No. 40,594	Lundberg, Steven W.	Reg. No. 30,568	Slifer, Russell D.	Reg. No. 39,838
Eliseeva, Maria M.	Reg. No. 43,328	Mack, Lisa K.	Reg. No. 42,825	Steffey, Charles E.	Reg. No. 25,179
Embretson, Janet E.	Reg. No. 39,665	Maki, Peter C.	Reg. No. 42,832	Terry, Kathleen R.	Reg. No. 31,884
Fogg, David N.	Reg. No. 35,138	Malen, Peter L.	Reg. No. P-44,894	Viksnins, Ann S.	Reg. No. 37,748
Fordenbacher, Paul J.	Reg. No. 42,546	Mates, Robert E.	Reg. No. 35,271	Woessner, Warren D.	Reg. No. 30,440

and also attorneys Michael L. Lynch (Reg. No. 30,871) and Lia M. Pappas (Reg. No. 34,095) of Micron Technology, Inc., as its attorneys with full power of substitution to prosecute this application and to transact all business in the Patent and Trademark Office in connection therewith.

The assignee certifies that the above identified assignment has been reviewed and to the best of the assignee's knowledge and belief, title is in the assignee.

Please direct all correspondence regarding this application to the following:

Schwegman, Lundberg, Woessner & Kluth, P.A.
Attn: Danny J. Padys
P.O. Box 2938
Minneapolis, MN 55402

Telephone: (612) 371-2109
Facsimile: (612) 339-3061

Dated: 7/24/1999

MICRON TECHNOLOGY, INC.

By: _____

Name: Michael L. Lynch

Title: Chief Patent Counsel

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

DECLARATION FOR PATENT APPLICATION

As a below named inventor I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:

PACKAGING OF ELECTRONIC CHIPS WITH AIR-BRIDGE STRUCTURES .

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56 (see page 3 attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, §119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

No such claim for priority is being made at this time.

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below:

No such claim for priority is being made at this time.

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application.

No such claim for priority is being made at this time.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of sole inventor : **Paul A. Farrar**
Citizenship: **United States of America** Residence: **So. Burlington, VT**
Post Office Address: 17 Yandow Drive
So. Burlington, VT 05403

Signature: Paul A. Farrar Date: 5/16/99
Paul A. Farrar

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

---

§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) it establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) it refutes, or is inconsistent with, a position the applicant takes in:

(i) opposing an argument of unpatentability relied on by the Office, or

(ii) asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.